ABSTRACT

A controller for a memory device and methods are provided. The controller has an updateable register bank adapted to send a first signal to an analog/memory core of the memory device for controlling operation of the analog/memory core. The analog/memory core has an array of flash memory cells and supporting analog access circuitry. A bus controller is coupled to the register bank. The bus controller is adapted to receive a second signal from the register bank and to send a third signal to the register bank for updating the register bank. A select register is coupled to the register bank. A processor is coupled to the bus controller and the select register.